Efficient Linearisation of Sigma-Delta Modulators using Single-Bit Dither

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Abstract

Idle tones and noise modulation in higher-order sigma-delta modulators (SDMs) can be eliminated using single-bit dither signals, with no additional reduction in dynamic range compared to multilevel dither signals. Unlike multilevel dither, single-bit dither is easily implemented in sigma-delta analogue-to-digital converters (ADCs).

Introduction

Sigma-delta modulation, where a single-bit quantiser is embedded within a negative feedback loop (Fig. 1), is now a commonly-used technique for implementing high-resolution analogue-to-digital and digital-to-analogue converters (DACs), principally because of a favourable insensitivity to component tolerancing [1]. Single-bit quantisation generates relatively high levels of quantisation noise, hence high resolution is achieved by oversampling and noise-shaping quantisation error away from the signal band. Loop filter *H* determines the noise-shaping characteristic of the modulator.

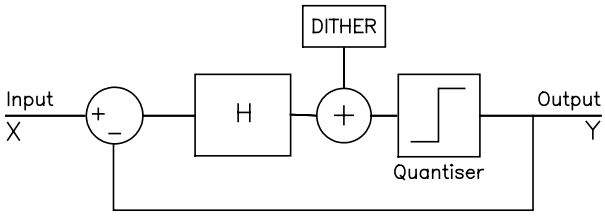

Fig. 1. General sigma-delta modulator.

Although the use of single-bit quantisers endows SDMs with good differential linearity, these systems can suffer from idle tones and noise modulation at low input-signal amplitudes, even for higher-order systems. Such errors are troublesome in a number of applications, for example in ADCs used for spectral analysis, and also in audio converters. They can be eliminated by dithering the modulator with a pseudo-random noise source applied at the quantiser input [2] (Fig. 1). Although dithering is relatively straightforward for SDM DACs, it is difficult to implement in ADCs using multilevel dither (i.e. dither signals that can assume a number of distinct values). We describe how sigma-delta modulators can be linearised using single-bit (two-level) dither, and present simulation results that suggest that to do so involves no additional signal-to-noise ratio (SNR) penalty compared to multilevel dither.

SDM Idle Tones

Ledzius and Irwin [3] have identified a relationship between idle-tone frequency and the DC input level x_{DC} applied to the modulator. For an SDM with quantiser levels ±1, sampling frequency f_s, baseband f_B and oversampling factor *OSF*, an important idle tone occurs at a frequency given by

$$f_{IT} = x_{DC} f_S = 2 x_{DC} f_B OSF .$$

Fig. 2(a) shows how the noise floor power spectrum of a fourth-order modulator changes as a DC input sweeps across the range 0 - 1/256. In this example *OSF* = 64 and f_B = 22 kHz. Idle tones at f_{IT} and $2f_{IT}$ can clearly be seen, increasing in frequency as the DC input increases.

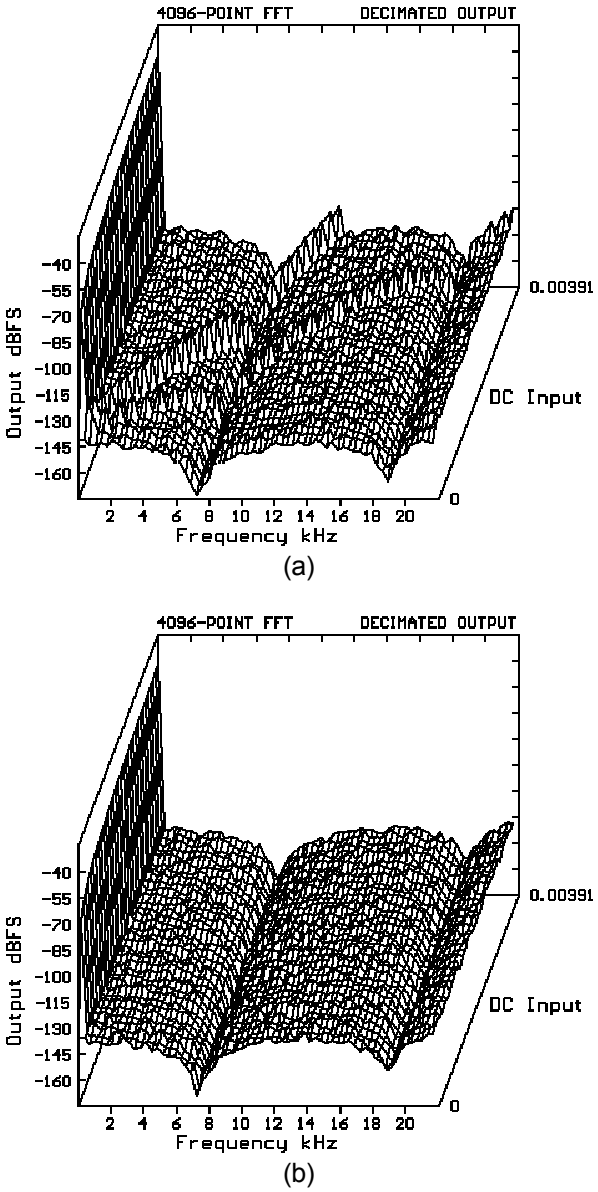

Fig. 2. DC-input sweep plots for 4th-order modulators.
(a) Undithered. (b) Dithered using 1-bit dither signals.

One-Bit Dither

Recent research has indicated two techniques that are capable of eliminating idle tones and noise modulation in sigma-delta systems. The modulator can be made *chaotic* by placing noise-shaping zeros outside the unit circle in the *z*-domain, although this approach has been shown to be costly in terms of SNR [4], [5]. Alternatively, *dither* can be introduced to the modulation process, which will have the effect

of randomly flipping samples in the quantiser output bitstream for quantiser input signals which are close to zero. This action can break up idle tones in sigma-delta modulators, linearising the process.

Whereas dither can easily be implemented in SDM DACs, the technique is more problematic in ADCs, where a random noise source which is stable with changes in temperature and supply voltage must be executed as an analogue process. Such difficulties can be overcome by quantising the dither to a single-bit signal prior to injection at the quantiser input, allowing simplified implementation. For example, single-bit dither can be added using a single switched capacitor, controlled by a random noise source generated in the digital domain. Alternatively it is possible to implement dither in the digital domain by using a 4-level quantiser and mapping the 4 output states to 2 levels, where flipping between the two states closest to zero can be controlled by a digital single-bit noise source.

In general, introducing dither reduces the dynamic range available from an SDM, because the addition of dither will both increase the total noise power within the loop and reduce modulator stability [4]. Given that 1-bit dithering of SDM ADCs is advantageous for the reasons outlined above, a series of simulations was performed to determine whether such an approach carries an additional SNR penalty compared to multilevel dither.

Simulations

64-times oversampled modulators with noise-shaping orders between 2 and 5 and with a range of dither amplitudes, were individually optimised to yield maximum dynamic range, using the approach described in [4]. The noise-shaping poles of each modulator were arranged in a Butterworth highpass configuration, while noise-shaping zeros were set to yield maximum baseband SNR; optimisation was achieved by controlling the cutoff frequency of the Butterworth poles. Dithered systems individually optimised for maximum dynamic range were simulated to determine the presence of unwanted baseband errors. A modulator was deemed ‘linear’ if two conditions were satisfied:

(i) no idle tones were visible in the baseband noise floor power spectrum across a range of DC input signals; the noise floor was examined using a 4096-point FFT,

(ii) baseband noise modulation was less than 1 dB for sinusoidal excitation across the dynamic range of the modulator.

Three dither amplitude distributions were investigated: single-bit quantised – i.e. bipolar probability distribution (BPD), rectangular probability distribution (RPD), and triangular probability distribution (TPD). For each distribution the minimum dither amplitude that successfully linearised the modulators was determined, and the associated SNR penalty relative to the undithered modulator noted.

Results

The results of the simulations are shown in Table 1. It is seen that the SNR penalty for linearising SDMs using dither remains approximately constant with changes in modulator order, with an average value of 5.5 dB. For higher-order systems (order > 2), single-bit (BPD) dither can successfully linearise sigma-delta modulators with no significant additional SNR penalty compared to RPD-dithered systems. However, for 2nd-order systems there appears to be an additional SNR penalty to pay for quantising the dither to one bit. We speculate that use of dither signals with many levels introduces an added degree of randomness to the dithering process, which can be of benefit when linearising simple (low-order) systems. The results also show that TPD dither carries a slightly higher SNR penalty compared to RPD dither.

Fig. 2(b) shows a noise-floor plot for a 4th-order modulator linearised using single-bit dither of amplitude ± 0.14 (determined by the optimisation process). No idle tones are visible, the power spectral density of the noise floor essentially being invariant with input signal characteristics.

Table 1. SNR penalties for dithered sigma-delta modulators.

Order	Undithered SNR_{pk} dB	Dithered SNR penalty dB		
		BPD	RPD	TPD
2	75.8	9.2	4.7	5.4
3	93.6	3.3	4.5	4.7
4	109.3	4.9	5.3	5.6
5	121.6	5.0	4.8	6.4

Conclusions

We have demonstrated that sigma-delta modulators can be efficiently linearised using dither which has been quantised to one bit, a technique which is relatively straightforward to implement in sigma-delta ADCs. For higher-order systems, the SNR penalty for linearisation with single-bit dither is no greater than that paid when using multilevel dither.

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